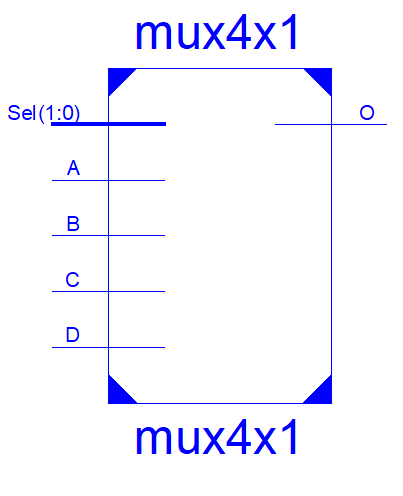
**EXPERIMENT 5**

**Aim:** Design of multiplexer based logic circuits.

**Exercise#1:** Design N-bit, 4-source common bus system shown in figure below in structural style of architecture using generic and for-generate statements. Use all inputs, outputs and selection lines in the form of bus.

**Design Code (MUX):**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

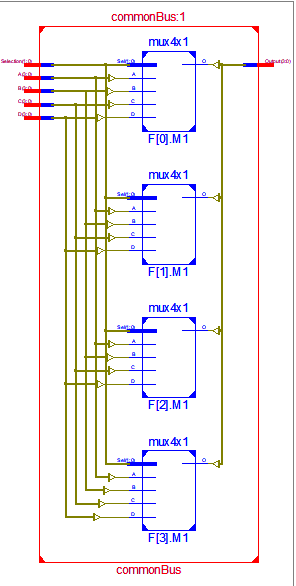
entity mux4x1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : in STD\_LOGIC;

D : in STD\_LOGIC;

 Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

O : out STD\_LOGIC);

end mux4x1;

architecture Dataflow of mux4x1 is

begin

O <= (not Sel(1) and (not Sel(0)) and A)

or (not Sel(1) and Sel(0) and B)

or (Sel(1) and (not Sel(0)) and C)

or (Sel(1) and Sel(0) and D);

end Dataflow;

**Design Code (Common Bus):**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity commonBus is

generic (n: integer := 4);

Port ( A,B,C,D : in STD\_LOGIC\_VECTOR (n-1 downto 0);

Selection : in STD\_LOGIC\_VECTOR (1 downto 0);

Output : out STD\_LOGIC\_VECTOR (n-1 downto 0));

end commonBus;

architecture Behavioral of commonBus is

component mux4x1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : in STD\_LOGIC;

D : in STD\_LOGIC;

Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

O : out STD\_LOGIC);

end component;

begin

F: for i in 0 to n-1 generate

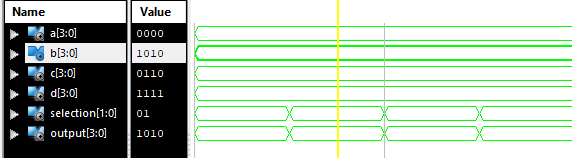
M1: Mux4x1 port map (A(i),B(i), C(i), D(i), Selection, Output(i));

end generate;

end Behavioral;

**Test Bench Code:**

A <= "0000";

B <= "1010";

C <= "0110";

D <= "1111";

Selection <= "00";

wait for 100 ns;

Selection <= "01";

wait for 100 ns;

Selection <= "10";

wait for 100 ns;

Selection <= "11";

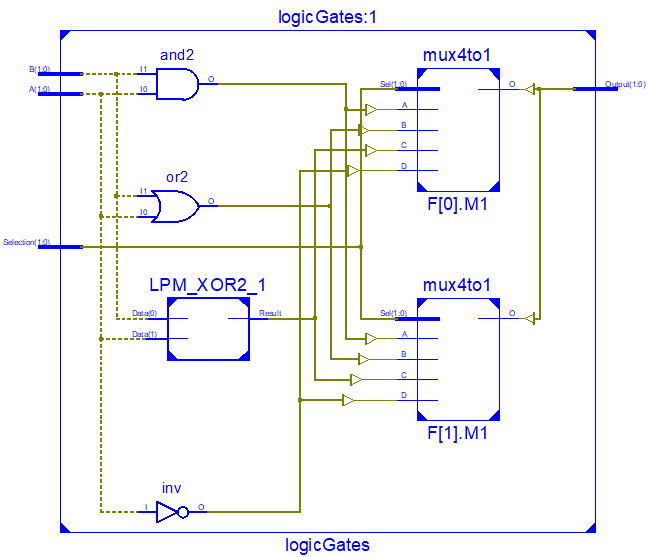
wait for 100 ns;

**Exercise#2:** Design N-bit logic circuit shown in figure below in structural style of architecture using generic and for-generate statements. Use all inputs, outputs and selection lines in the form of bus.

**Design Code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;



entity logicGates is

generic (n: integer := 2);

Port ( A,B : in STD\_LOGIC\_VECTOR (n-1 downto 0);

Selection : in STD\_LOGIC\_VECTOR (1 downto 0);

Output : out STD\_LOGIC\_VECTOR (n-1 downto 0));

end logicGates;

architecture Behavioral of logicGates is

component mux4to1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : in STD\_LOGIC;

D : in STD\_LOGIC;

Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

O : out STD\_LOGIC);

end component;

signal S1, S2, S3, S4 :STD\_LOGIC\_VECTOR (n-1 downto 0);

begin

F: for i in 0 to n-1 generate

S1(i) <= A(i) and B(i);

S2(i) <= A(i) or B(i);

S3(i) <= A(i) xor B(i);

S4(i) <= not(A(i));

M1: Mux4to1 port map (S1(i),S2(i),S3(i), S4(i), Selection, Output(i));

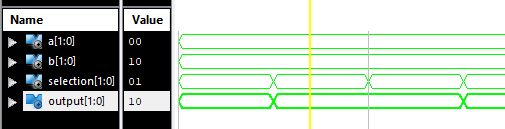
end generate;

end Behavioral;

**Test Bench Code:**

A <= "00";

B <= "10";



Selection <= "00";

wait for 100 ns;

Selection <= "01";

wait for 100 ns;

Selection <= "10";

wait for 100 ns;

Selection <= "11";

wait for 100 ns;

**Exercise#3:** Design N-bit shift circuit in using behavioural style of architecture which performs four operations given in table. Use all inputs, outputs and selection lines in the form of bus.